RELIABILITY ANALYSIS OF THE LOCK-IN THERMOGRAPHY PROCESS FOR DEFECTS CHARACTERIZATION ON A THROUGH-SILICON VIA (TSV) BASED THREE-DIMENSIONAL INTEGRATED CIRCUIT

Ji Yong Bae, Kye-Sung Lee, Hwan Hur, Geon-hee Kim, Ki Soo Chang
Division of Scientific Instrumentation
Korea Basic Science Institute
169-148 Gwahak-ro, Yuseong-gu, Daejeon, Republic of Korea 34133
E-mail : baejy@kbsi.re.kr

KEY WORDS: Lock-in thermography, Non-destructive evaluation, Finite element analysis

The use of the lock-in thermography (LIT) as a non-destructive evaluation technique is becoming increasingly attractive for detecting and characterizing the defects such as the shorts and resistive opens in 3D package or stacked IC [1,2]. According to this trend, the reliability study of the LIT process for various types of defects is essentially required to confirm and validate the sensitivity. In this study, we developed the 3D FE model of TSV structure with 4 silicon chip integration, and experimentally validated our FE model using measured current–voltage (I–V) and lock-in thermography (LIT) measurements. From the finite element analysis, the thermal distributions in the TSV model and phase angle for the lock-in frequency are calculated and compared according to various types of defects.

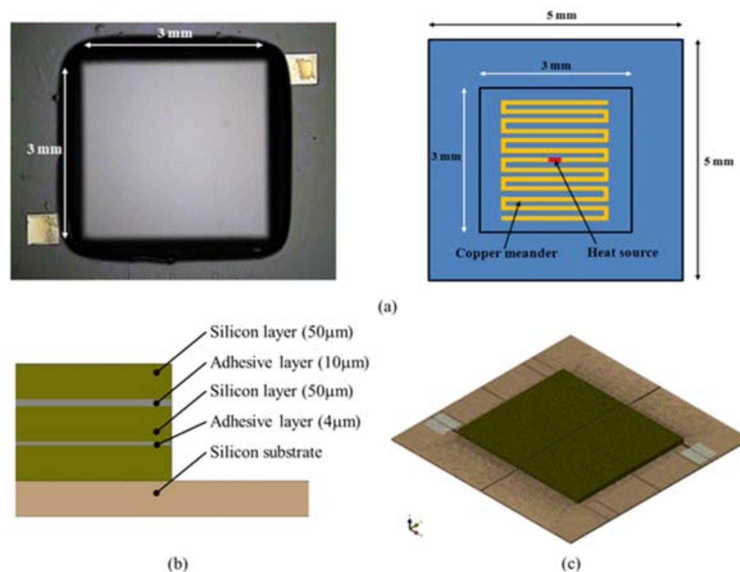

Figure 1. (a) 3-layer stacked-wafer specimen, (b) geometric model of 3-layer stacked-wafer specimen and (c) its FE model

References;

[1] C. Schmidt et al., “Application of lock-in thermography for failure analysis in integrated circuits using quantitative phase shift analysis,” *Mater. Sci. Eng. B,* **177**, 1261-12670 (2012).
[2] Y Li et al., “A Review of Failure Analysis Methods for Advanced 3D Microelectronic Packages”, *J. Electron. Mater.,* **45(1)**, 116-124 (2016)